

# Thomas W. Gustin

# Resume'

## FUNCTIONAL SUMMARY

Highly self-motivated independent (freelance) senior (hardware) design engineer and company owner with 31+ years experience in all phases of chip, board, and systems level product development. Worked for three different Research and Development companies for 20 years (1976⇒1996), and have been operating as a contract electronic engineering services business doing business as (dba) GUSTECH ever since. Some of the technological experience includes: system-level through detail design of analog, digital, and mixed signal circuits and parallel bus speeds up to 80MHz, a custom analog hybrid, an ASIC using 0.8-micron CMOS technology, many embedded 4/8/12/16/32-bit microprocessor-based and DSP designs (hardware design and assembly-level programming), a wide variety of programmable devices (CPLD's & FPGA's) using schematic capture and VHDL design entry with comprehensive simulations, vast spectrum of sizes and speeds of real-time sequential state machines, with most programs utilizing the current leading-edge technology. Have recently expanded the contract electronic engineering services to include 2 & 4-layer printed circuit board layout (*more layers coming*) to enable functioning as a "one-stop-shop." Have considerable technical proficiency in data acquisition, instrumentation, sensor/actuator interfacing, from simple, one-of-a-kind custom solutions through large-scale multi-million dollar cockpit I/O systems, including the successful launch of two full-featured I/O board-level product lines. One other note: I have been working harder as an independent contract engineer than I ever did the first 20 years of my career, and enjoying it much more also.

## RELEVANT SKILLS

SKILL	Years	SKILL	Years	SKILL	Years
Electronic Hardware, Systems, Circuit Design	31+	Schematic Capture (by hand & CAE tools), Detailed Design	31+	Rapid-Prototyping, Custom Test Systems	31+
Data Acquisition Systems, Modules, Boards	25+	Custom Analog Control Circuits, Sensing, Interfacing...	31+	Technical Writing, Publishing, Presentations	25+
Project/Product Planning	31+	Technical Design Reviews	31+	Product Documentation	31+
Technical Research/Reports	31+	Embedded CPU's & DSP's	31+	ASIC, PLD, FPGA Design	20+
VHDL Design & Test	17+	Assembly-level coding	31+	CMOS Digital Designs	31+
Network Interface Cards	19+	I/O IPack Mezzanine Modules	15+	Project/Program Proposals	25+
Technical Training	20+	College (Senior Project) Mentoring	15+	Printed Circuit Board Layout/Design	4+

There are many more details on my web site regarding these and other skills, various technologies, and typical planning, research, design, writing, and training services I regularly execute, including many examples of past work.

## EXPERIENCE

**GUSTECH, 1996-Present:** Independent Senior Design Engineer, Owner, Tech-Writer-Trainer; Xenia, Ohio.

Have been conducting business as an independent (freelance) senior design engineer providing contract electronic engineering design services *dba* GUSTECH since mid-1996. Over that period, many different clients have received a wide range of design services, from conceptual and preliminary designs through the launch of an entire I/O product line, including its "flagship" premiere products. The majority of my work has been for many different contracts for assorted Government Agencies, including numerous SBIR and STTR research projects for the Air Force, Navy and Army, and other (unnamable agencies). All of these projects were either classified or covered by long-duration non-disclosure agreements that prevent disclosing project details, client names and contact information. Client anonymity is fully enforced.

Many of the contract electronic engineering design services have been conducted as firm-fixed-fee (FFF) contracts (Proposal, Purchase Order, Invoices → 1099's), while other more "fluid" consulting services have been conducted as Time and Material (T&M) contracts (Purchase Order and Invoices → 1099's).

Recent research activities have evolved into functional applications utilizing RFID, passive power sources like Electrochemical Double Layer Capacitors (EDLCs), MEMs, Sensors, Anti-Tamper protection techniques for sensitive Intellectual Property

within embedded systems, and an online (downloadable design files available on my web site) next-generation, highly-integrated, autonomous data acquisition system design. Majority of recent designs have been custom test platforms, most with large CPLD or FPGA controllers, used as semi-automatic test equipment or as proof-of-concept exercisers.

For most of the GUSTECH customers, varying degrees of design depth have been provided for ISA, PCI, PMC, PC-104 and the IP Module mezzanine buses. For one of those same customers, embedded CPU designs were executed using the 68302, and the 68705 CPUs. Assembly level programming was used for all of the computers and all of the embedded CPU designs. The largest most recent design was a quad-Opteron (SledgeHammer) Blade (115 D-size schematic sheets) using 48volt supply with multi-tiered power distribution, Hyperchannel links, DDR memory banks, and an extensive SMBus-based status and control instrumentation system for all power and environmental parameters and conditions.

Many recent projects are modernization tasks of older systems facing end-of-life issues with components, converting boards of logic to a single FPGA or CPLD, updating analog circuits, incorporating newer power management designs, etc.

**GUSTECH, 2000-2004:** as a part time contracted Technical Instructor for Solution Technology.

Provided contracted on-site educational services for Solution Technology, the best-in-class training company for storage-related hardware and protocols like SCSI, iSCSI, Fibre Channel, SAS, and much more. Have provided 2, 3, 4, and 10-day on-site training sessions over 86 different trips (including: London, Singapore, and Bangalore) to 1,545 students since 2000, specializing in short Fibre Channel courses, and really intense SCSI and iSCSI classes. Some course critique comments are viewable on my web site. I am still available to provide technical training through Solution Technology should the need arise.

**Systran Corporation, 1989-1996:** Dayton, Ohio {now out of business}.

Developed business plan for launch of new I/O product line of standardized IP Modules, including market and competitive analyses, and developed the features and functions for the first series of about 50 products. Led a small team that successfully engineered into production 22 of the generic mezzanine I/O interface boards with several of their carriers and supporting test hardware, test and application software, and complete user documentation. Also developed several high-speed interfaces for 150MHz fiber-optic shared-memory-network. Introduced and developed top-down program planning techniques which were instrumental in establishing rigorous design and review methodologies for ISO-9001 certification. Used ViewLogic CAE with VHDL, schematic capture, synthesis, digital simulation, EPLD targeting, and many other advanced development techniques for the majority of the digital design, and all of the analog design work.

**Systems Research Laboratories (SRL), 1978-1989:** Dayton, Ohio {now out of business}.

Supported research efforts of the Air Force's Aeronautical Systems Division, Life Support System's Program Office, Crew Escape Technology Advanced Development Program Office, and the Armstrong Aerospace Medical Research Laboratory (formerly AFAMRL). Several custom Data Acquisition Systems were also developed for the Aircrew Systems Department of The Navel Air Test Center in Patuxent River, Maryland. A few of the dozens of programs included:

- ◆ The Solid State Memory Instrumentation Recorder (SSMIR) {*responsible for all phases of design and led team in implementation of* retrofit of a PCM/Telemetry data acquisition system within a manikin with non-volatile "Bubble-Memory" technology;
- ◆ The Solid State Physiological In-flight Data Recorder (SSPIDR) {*responsible for all phases of design and prototype implementation of* a self-contained 16 channel biomedical and environmental data acquisition system;
- ◆ The Boom Event Analyzer Recorder (BEAR) {*responsible for all phases of design and prototype implementation of* an unconstrained sound detection analysis system with a real-time signature discriminator and non-volatile recording;
- ◆ The Limb Restraint Evaluator (LRE) {*responsible for all phases of design and implementation of* a 96-channel, PCM-based data acquisition system with custom sensor analog interface circuits and an on-board solid-state non-volatile memory and telemetry retrieval systems;
- ◆ Advanced Dynamic Anthropomorphic Manikins (ADAM) {*responsible for all phases of design and prototype implementation of* an unconstrained, non-volatile, 128 channel, 8-bit, 1000 samples/second/channel data acquisition system including a custom analog sensor interface Hybrid within a ruggedized manikin for the CREST program;
- ◆ Durable Electronic Logging Violent Event Recorder (DELVER) {*responsible for all phases of design and implementation of* 10000 samples/second/channel, low-power, unconstrained, modular, non-volatile, data acquisition logging system (*applied embodiment for 2 patents*);
- ◆ Many other smaller programs and projects including several large (100+ pages) trade and technology studies directly related to data acquisition systems, PCM & telemetry systems, state-of-the-art devices, etc.

For AFAMRL, supported research efforts for the Generic Avionics System Simulator (GASS) {*responsible for all phases of design and implementation of* project preparing a B-52G Simulator for human factors workload studies, including all cockpit instrumentation, 32-bit minicomputer's I/O interfaces, custom DMA communications links between dissimilar mini-computers, generic hydraulic force loader system design/build, and I/O systems upgrades and maintenance.

For SRL's Autometrix Division, supported all (analog, digital, and CPU) hardware and software aspects of entire microcomputer-based electro-optical gauging and industrial control systems product line, including the first (company-wide) successful fielding of all-CMOS-based designs in industrial applications (1978).

**ACD Corporation, 1976-1978:** Dayton, Ohio {now out of business}.

Designed, built, documented, and tested many different types and sizes of analog and digital circuits and systems, specializing in the (*then new*) CMOS technology (4000 series), including standard (the very first IC-CPU) 4-bit (Intel 4004), 8-bit (8008, 8080) and a custom bit-sliced 12-bit microcomputer-based machine, and many custom digital sequential state machines and analog interface circuits usually configured as standalone products or semi-automatic test equipment. Also involved in the design and successful fielding of a battery-powered Baudot-code portable terminal using thermal printing, hall-effect keyboard, scores of CMOS logic, low EMI balanced circuits, and primitive encryption technology.

**United States Air Force; 1972-1975:**

Honorable Discharge. Strategic Air Command; 381<sup>st</sup> Communications Squadron: ICBM: TITAN-II Missiles at Holloman Air Force Base.

## PAPERS & PUBLICATIONS

Have provided technical (*shadow*) writing for three large technology survey publications, and for three different papers presented by other (*Managers*) people. Wrote, published, and presented two different papers for the LRE program, three different papers for the ADAM program, two for the DELVER program, a complete tutorial (½ day seminar) on data acquisition system design tradeoffs, and a paper/article on real-time data distribution of telemetry information using shared memory networking techniques. Have also written dozens of technical notes and application notes, as well a various depths of user's manuals for most of the products developed. Have also written the base-line text for two different Patent Applications. Paper presentations have occurred at: four different Sensors Expos, two National Aerospace and Electronics Conferences, two SAFE Symposiums, three International Telemetry Conferences, and one at the Instrument Society of America show. Have also prepared a complete book outline as a result of the invitation by the Acquisitions Editor of Longman Scientific & Technical (publishers) to author a book on Data Acquisition/Interfacing topics. Some of these documents are downloadable from my web site: [www.gustech.biz](http://www.gustech.biz).

## EDUCATION SUMMARY

Brunnerdale Seminary (1965-1969), College Preparatory High School (radio club, audio/visual department services). Wright State University, University of Dayton, Sinclair Community College, Community College of the Air Force, Wichita State University, and the Capitol Radio Engineering Institute, (total 1969-1985) culminating in 275 quarter hours in Electrical Engineering, Electrical Engineering Technology, and some Management programs.

In addition to the "institutional" studies, many mini-courses and seminars have been attended, some earning CIU credits, covering project and program management techniques, but most covering technology and specific applications. These varied from three weeks of intensive training on SelBUS super-mini-computers, two weeks of ViewLogic VHDL and schematic capture design and simulation techniques, down to dozens of one day seminars covering topics like avoiding pitfalls in designing data acquisition systems, proper design for high density surface mount technology, designing for maximum DSP performance, design for testability, design for error-free synthesis, quality assurance techniques, no-slippage project planning techniques, technical supervision skills, etc.

Two other notes regarding education: 1) it is always ongoing; every project is a multi-faceted-dimensional learning experience; and 2) I continue to contribute my time providing College Mentoring services for Senior Class Electronic Engineering Projects at a couple of local Universities.

## WEB SITE

My Web Site: [www.gustech.biz](http://www.gustech.biz) is designed to present supplemental information for this too-brief resume', with many research, planning, design, technical writing, and training services' descriptions and examples providing details only hinted at in this document, or not covered at all. Current "public" activities include the online design of the **SER**: Shock Event Recorder, with all design documents being downloadable.