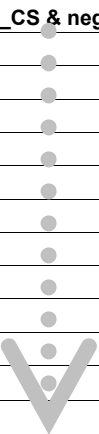


66 State Gray Code Counter based 3 Byte SPI Write Sequence

HEX	b6	b5	b4	b3	b2	b1	b0	Decimal Count:	State function: Function is decoded during and implemented at END of state and is active during next count state
00	0	0	0	0	0	0	0	1	NO OPERATION at count Zero
01	0	0	0	0	0	0	1	2	Negate (high) n_CS & negate (low) SCL <i>just to make sure</i>
03	0	0	0	0	0	1	1	3	Assert (low) n_CS
02	0	0	0	0	0	1	0	4	DeviceID(3) -> SI {='0'}
06	0	0	0	0	1	1	0	5	Assert (high) SCL {clocks SI into X9271} [1]
07	0	0	0	0	1	1	1	6	Negate (low) SCL & DeviceID(2) -> SI {='1'}
05	0	0	0	0	1	0	1	7	Assert (high) SCL {clocks SI into X9271} [2]
04	0	0	0	0	1	0	0	8	Negate (low) SCL & DeviceID(1) -> SI {='0'}
0C	0	0	0	1	1	0	0	9	Assert (high) SCL {clocks SI into X9271} [3]
0D	0	0	0	1	1	0	1	10	Negate (low) SCL & DeviceID(0) -> SI {='1'}
0F	0	0	0	1	1	1	1	11	Assert (high) SCL {clocks SI into X9271} [4]
0E	0	0	0	1	1	1	0	12	Negate (low) SCL & BusAdd(3) -> SI {='0'}
0A	0	0	0	1	0	1	0	13	Assert (high) SCL {clocks SI into X9271} [5]
0B	0	0	0	1	0	1	1	14	Negate (low) SCL & BusAdd(2) -> SI {='0'}
09	0	0	0	1	0	0	1	15	Assert (high) SCL {clocks SI into X9271} [6]
08	0	0	0	1	0	0	0	16	Negate (low) SCL & BusAdd(1) -> SI {='0' or '1'}
18	0	0	1	1	0	0	0	17	Assert (high) SCL {clocks SI into X9271} [7]
19	0	0	1	1	0	0	1	18	Negate (low) SCL & BusAdd(0) -> SI {='0' or '1'}
1B	0	0	1	1	0	1	1	19	Assert (high) SCL {clocks SI into X9271} [8]
1A	0	0	1	1	0	1	0	20	Negate (low) SCL & InsOpCode(3) -> SI {='1'}
1E	0	0	1	1	1	1	0	21	Assert (high) SCL {clocks SI into X9271} [9]
1F	0	0	1	1	1	1	1	22	Negate (low) SCL & InsOpCode(2) -> SI {='0' or '1'}
1D	0	0	1	1	1	0	1	23	Assert (high) SCL {clocks SI into X9271} [10]
1C	0	0	1	1	1	0	0	24	Negate (low) SCL & InsOpCode(1) -> SI {='0' or '1'}
14	0	0	1	0	1	0	0	25	Assert (high) SCL {clocks SI into X9271} [11]
15	0	0	1	0	1	0	1	26	Negate (low) SCL & InsOpCode(0) -> SI {='0'}
17	0	0	1	0	1	1	1	27	Assert (high) SCL {clocks SI into X9271} [12]
16	0	0	1	0	1	1	0	28	Negate (low) SCL & RegAdd(1) -> SI {='0' or '1'}
12	0	0	1	0	0	1	0	29	Assert (high) SCL {clocks SI into X9271} [13]
13	0	0	1	0	0	1	1	30	Negate (low) SCL & RegAdd(0) -> SI {='0' or '1'}
11	0	0	1	0	0	0	1	31	Assert (high) SCL {clocks SI into X9271} [14]
10	0	0	1	0	0	0	0	32	Negate (low) SCL & BankAdd(1) -> SI {='0' or '1'}
30	0	1	1	0	0	0	0	33	Assert (high) SCL {clocks SI into X9271} [15]
31	0	1	1	0	0	0	1	34	Negate (low) SCL & BankAdd(0) -> SI {='0' or '1'}
33	0	1	1	0	0	1	1	35	Assert (high) SCL {clocks SI into X9271} [16]
32	0	1	1	0	0	1	0	36	Negate (low) SCL & NVdataOut(7) -> SI {='0' or '1'}
36	0	1	1	0	1	1	0	37	Assert (high) SCL {clocks SI into X9271} [17]
37	0	1	1	0	1	1	1	38	Negate (low) SCL & NVdataOut(6) -> SI {='0' or '1'}
35	0	1	1	0	1	0	1	39	Assert (high) SCL {clocks SI into X9271} [18]
34	0	1	1	0	1	0	0	40	Negate (low) SCL & NVdataOut(5) -> SI {='0' or '1'}
3C	0	1	1	1	1	0	0	41	Assert (high) SCL {clocks SI into X9271} [19]
3D	0	1	1	1	1	0	1	42	Negate (low) SCL & NVdataOut(4) -> SI {='0' or '1'}
3F	0	1	1	1	1	1	1	43	Assert (high) SCL {clocks SI into X9271} [20]
3E	0	1	1	1	1	1	0	44	Negate (low) SCL & NVdataOut(3) -> SI {='0' or '1'}
3A	0	1	1	1	0	1	0	45	Assert (high) SCL {clocks SI into X9271} [21]
3B	0	1	1	1	0	1	1	46	Negate (low) SCL & NVdataOut(2) -> SI {='0' or '1'}
39	0	1	1	1	0	0	1	47	Assert (high) SCL {clocks SI into X9271} [22]
38	0	1	1	1	0	0	0	48	Negate (low) SCL & NVdataOut(1) -> SI {='0' or '1'}

66 State Gray Code Counter based 3 Byte SPI Write Sequence

28	0	1	0	1	0	0	0	0	49	Assert (high) SCL {clocks SI into X9271} [23]
29	0	1	0	1	0	0	1	1	50	Negate (low) SCL & NVdataOut(0) -> SI {'0' or '1'}
2B	0	1	0	1	0	1	1	1	51	Assert (high) SCL {clocks SI into X9271} [24]
2A	0	1	0	1	0	1	0	0	52	Negate (low) SCL
2E	0	1	0	1	1	1	0	0	53	Negate (high) n_CS & negate (low) SCL
2F	0	1	0	1	1	1	1	1	54	
2D	0	1	0	1	1	0	1	55		
2C	0	1	0	1	1	0	0	56		
24	0	1	0	0	1	0	0	57		
25	0	1	0	0	1	0	1	58		
27	0	1	0	0	1	1	1	59		
26	0	1	0	0	1	1	0	60		
22	0	1	0	0	0	1	0	61		
23	0	1	0	0	0	1	1	62		
21	0	1	0	0	0	0	1	63		
20	0	1	0	0	0	0	0	64		
60	1	1	0	0	0	0	0	0	65	
40	1	0	0	0	0	0	0	0	66	Negate (high) n_CS & negate (low) SCL
back to count = 00hex										
HEX	b6	b5	b4	b3	b2	b1	b0	Decimal Count:	State function: Function is decoded during and implemented at END of state and is active during next count state	
SPECIAL NOTE: Not all write operations require the 10mS High Voltage Non-volatile write cycle, which is why it is handled in a different (looping) module; while, all operations require a 2uS n_CS negation.										

Guarantees 2uS minimum
Chip Select Negation Time
between writes;
see Special Note Below